

<b>Notice of References Cited</b>	Application/Control No. 10/802,885	Applicant(s)/Patent Under Reexamination MURATA ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,815,126 B2	11-2004	Fey et al.	430/9
	B	US-5,235,139	08-1993	Bengston et al.	174/257
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ning-Cheng Lee, "Lead-Free Chip-Scale Soldering of Packages," Chip Scale Review (March - April, 2000), pp. 1 - 6.
	V	Jennie S. Hwang and Zhenfeng Guo, "Effects of Pb Contamination on the Material Properties of Sn/Ag/Cu Solder," Chip Scale Review (January - February, 2001), pp. 1-5.
	W	Y. M. Chow, W.M. Lau, and Z.S. Karim, "Surface Properties and Solderability Behaviour of Nickel- Phosphorous and Nickel-Boron Deposited by Electroless Plating," Surf. Interface Anal. Vol. 31, (2001) pp.321-327.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.